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EXAMINER	
DILLER, JESSE DAVID	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,402	CYPHER ET AL.	
	Examiner	Art Unit	
	Jesse Diller	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9-14 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12* is/are allowed.

6)☒ Claim(s) *1-4,6-11,13,14 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Examiner acknowledges the receipt of the amendment in response to the office action dated 03/14/2006 which amendment was received 03/23/2006. At this point, claims 1, 6, 12-13, and 16 have been amended and claims 5 and 15 have been cancelled. Thus, claims 1-4, 6-14, and 16-24 are still pending in the application.

Objections to the disclosure

2. In response to amendment, the objection to the specification is withdrawn.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 11, 13, 21, 22, 23, and 24 have been fully considered.

4. As for Applicant's arguments regarding the rejection of claims by Hagersten '671, Applicant claims that the mode unit is not separate from the memory. However, while the partial directory cache 950 of Fig. 10 is clearly separate from both the processor subsystem and the memory module, being connected to the network interface. However, because the system of Hagersten '671 utilizes a shared memory (i.e., 204a-b, Fig. 2 and 704, Fig. 10), the request is visible to the memory subsystem. **Therefore, this rejection is withdrawn.**

5. As for Applicant's arguments regarding the rejection of claims by Martin, Applicant claims that the mode unit is not separate from the processing subsystem.

This is correct; while the cache controller circuitry that performs the function of the mode unit may be taken to be part of the network, it is not separate from the processing subsystems. **Therefore, this rejection is withdrawn.**

6. However, the Examiner is confused by the arguments on Page 12, 4th par. Applicants claim that "the mode unit is also configured to receive a given coherency request initiated by a requesting processing subsystem and not visible to other processing subsystems or the memory subsystem." However, claim 1 as recited in the paragraph directly preceding this argument recites that the receiving and controlling steps are performed by the network, not the mode unit. This is also echoed in the difference/confilict between claims 1 and 16; claim 1 recites that the network receives and controls the request and its transmission, while claim 16 says that the mode unit is configured to perform these steps.

Clarification/correction of this issue is required.

In any case, please see the following new rejections, which render moot the arguments.

7. Claims 1-4, 6-7, 13-14, 16-17 are rejected under 35 U.S.C. 103(a) as being anticipated by Martin et al, US Patent application #10,037,727, published September 19, 2002 as Publication # US 2002/0133674 A1 in view of Hagerstein, published European Patent Application EP 0 817 069 A1 (not to be confused with Hagersten, US Patent 5,864,671).

8. As for claims 1, 16, Martin teaches:

- A multiprocessing system (Pg. 3, Par. 44, line 1) comprising:
- A plurality of processing subsystems (12a-f, Fig. 1; Pg. 3, Par. 44, line 2-3), each including a cache memory (22, Fig. 1; Pg. 3, Par. 45, line 2);
- A memory subsystem (16, Fig. 1; Pg. 3, Par. 44, lines 8-9) including a directory (21, Fig. 1; Pg. 3, Par. 44, line 10);
- A network interconnecting said plurality of processing subsystems and said memory subsystem (14, Fig. 1; Pg. 3, Par. 44, line 3)
- A mode unit (26, Fig. 1); wherein the network is configured to:
- receive a given coherency request initiated by a requesting processing subsystem (Par. 13, lines 5-6); wherein
- Coherency requests do not specify whether said given coherency request is transmitted through said network according to said directory protocol or said broadcast protocol (Page 4, Par. 61, lines 4-6 teach that the protocol indication is determined by circuitry hardwired into the memory controller, not programmed into a request); and

- when said coherency request is transmitted through said network according to said directory protocol (Page 3, Par. 51, lines 1-3), said given coherency request is transmitted through said network to said memory subsystem. (Page 3, Par. 51, line 3 teaches that the request is transmitted to the directory; Pg 2, Par. 44, lines 8-10 teach that the directory is included in the memory subsystem).
- Martin also teaches that when the mode unit receives the request, it is not visible to other processors or the memory. This is because the protocol mode unit is part of the processor system. The processor sends the request to the mode unit which determines the protocol. Then, according to Par. 13, the request is sent directly to the appropriate receiver. The other processors and memory do not snoop the request prior to the protocol determination.

9. **Martin does not expressly teach that:**

- the network includes the mode unit separate from the processing subsystems and the memory, or that
- the network controls the transmission protocol.

10. **Hagerstein discloses** a multiprocessing computer system which includes a plurality of processing units (102-106, Fig. 2), each including a cache memory (114, Fig. 1) a shared memory (110, Fig. 2), a network (108, Fig. 1) connecting the components, and a coherence transformer (i.e., mode storage unit) which determines the transmission protocol (200, Fig. 2; Fig. 7A). Hagerstein's system uses multiple coherency protocols depending on several indications, including whether a coherency request is directed toward a line stored in the coherency transformer. Hagerstein

teaches that the coherence transformer stores the states of certain cache lines and based on the state of the cache lines in the transformer and the presence or absence of cache lines in the transformer, the system will either answer the coherence request by using a broadcast protocol or a Mtag protocol (which is similar to a directory protocol). See Page 3, lines 40 and 49-54. The coherence transformer is included in the network, not the processing elements (Fig. 2).

11. At the time of the invention it would have been obvious to a person of ordinary skill in the art who has read the disclosures of both Martin and Hagerstein to modify the system of Martin by centralizing the protocol determining circuitry in Martin's cache controllers into the network, as does Hagerstein. This system would allow the system to include only one protocol determination circuit (i.e., mode unit). The processing subsystems would send their requests to the mode unit, and as in Par. 13, the request would be forwarded by the network directly to the correct receiver. In this setup, the mode unit would receive the request (e.g., input to 29, Fig. 4, Martin) and indicate the proper protocol, thereby controlling the protocol used.

12. The motivation for doing so is taught by Hagerstein on Page 4, line 58 – Page 5, line 2, namely that a centralized coherence transformer allows external processing elements that may have different protocols or bus speeds to access the system. Additionally, centralizing the circuitry significantly decreases the amount of circuitry needed to realize the use of the system.

13. Therefore, it would have been obvious to combine the centralized coherence transforming circuitry of Hagerstein with the system of Martin, for the benefits above, to obtain the invention as specified in claim 1.

14. **As for claim 2**, Martin and Hagerstein teach the limitations of claim 1, and additionally teaches:

- The directory (21, Fig. 1; Pg. 3, Par. 44, line 10) includes a plurality of entries corresponding to different memory locations mapped to said memory subsystem (Pg. 3, Par. 46, lines 4-6), wherein:
- Each entry contains information indicative of whether a cached copy of a corresponding block has been created in one or more of said plurality of processing subsystems (Pg. 3, Par. 46, lines 4-7).

15. **As for claim 3**, Martin and Hagerstein teach the limitations of claim 2, and additionally teaches:

- When a coherency request is transmitted through said network (Pg. 3, Par. 47, lines 1-4) according to said broadcast protocol, said coherency request is broadcasted to said memory subsystem and to each of said plurality of processing subsystems regardless of information contained within said directory (Pg. 3, Par. 50, lines 1-3, 5-10).

16. **As for claim 4**, Martin and Hagerstein teach the limitations of claim 3, and additionally teaches:

- Said given coherency request is initiated by a requesting processing subsystem, and wherein said given coherency request is transmitted to said network through

a point-to-point link (Claim 1(a) teaches initiation from a processor unit and that the request is transmitted directly from one PU to another, i.e., point-to-point network. Also see Fig. 1 for PTP connection between PU 12a and network 14).

17. **As for claim 6, Martin teaches**:

- That when said coherency request is transmitted through said network according to said directory protocol (Page 3, Par. 51, lines 1-3),
- Said given coherency request is transmitted through said network to said memory subsystem. (Page 3, Par. 51, line 3 teaches that the request is transmitted to the directory; Pg 2, Par. 44, lines 8-10 teach that the directory is included in the memory subsystem),
- An entry in said directory is accessed by said memory subsystem (Page 3, Par. 51, lines 4-7), and
- Responsive coherency commands are provided to one or more of said plurality of processing subsystems dependent upon information contained within said directory (Page 3, Par. 51, lines 8-10).

18. **As for claims 7 and 17, Martin teaches**:

- A coherency mode storage unit (26, Fig. 1) configured to store an indication (42, Fig. 4; see also Pg. 3, Par. 57) to control whether a given coherency request is transmitted through said network according to a directory protocol or a broadcast protocol (Pg. 3, Par. 52); (While Martin does not name this unit a coherency mode storage unit, the cache controller he discloses performs the function of the mode unit disclosed by the instant application).

19. **As for claim 13**, Martin teaches:

- A method of operating a multiprocessing system (Pg. 3, Par. 44, line 1) including a plurality of processing subsystems (12a-f, Fig. 1; Pg. 3, Par. 44, line 2-3) and a memory subsystem (16, Fig. 1; Pg. 3, Par. 44, lines 8-9) interconnected through a network (14, Fig. 1; Pg. 3, Par. 44, line 3), the method comprising:
- A mode unit (26, Fig. 4)receiving a coherency request (see 29, Fig. 4) and indicating (50, Fig. 4) whether the request is transmitted through said network according to a directory protocol or a broadcast protocol (Pg. 3, Par. 52);
- Said network conveying said coherency request according to said indication (Page 3, Par. 50, lines 1-7 teach that a request is transmitted by the network according to an indication that the request should be transmitted by a broadcast protocol);
- That when said coherency request is transmitted through said network according to said directory protocol (Page 3, Par. 51, lines 1-3),
- Said given coherency request is transmitted through said network to said memory subsystem. (Page 3, Par. 51, line 3 teaches that the request is transmitted to the directory; Pg 2, Par. 44, lines 8-10 teach that the directory is included in the memory subsystem), and an entry in said directory is accessed by said memory subsystem (Page 3, Par. 51, lines 4-7);
- Martin also teaches that when the mode unit receives the request, it is not visible to other processors or the memory. This is because the protocol mode unit is part of the processor system. The processor sends the request to the mode unit

which determines the protocol. Then, according to Par. 13, the request is sent directly to the appropriate receiver. The other processors and memory do not snoop the request prior to the protocol determination.

20. Martin does not expressly teach that the network includes the mode unit, that the mode unit is separate from the processors and memory subsystems.

21. Hagerstein discloses a multiprocessing computer system which includes a plurality of processing units (102-106, Fig. 2), each including a cache memory (114, Fig. 1) a shared memory (110, Fig. 2), a network (108, Fig. 1) connecting the components, and a coherence transformer (i.e., mode storage unit) which determines the transmission protocol (200, Fig. 2; Fig. 7A). Hagerstein's system uses multiple coherency protocols depending on several indications, including whether a coherency request is directed toward a line stored in the coherency transformer. Hagerstein teaches that the coherence transformer stores the states of certain cache lines and based on the state of the cache lines in the transformer and the presence or absence of cache lines in the transformer, the system will either answer the coherence request by using a broadcast protocol or a Mtag protocol (which is similar to a directory protocol). See Page 3, lines 40 and 49-54. The coherence transformer is included in the network, not the processing elements (Fig. 2).

22. At the time of the invention it would have been obvious to a person of ordinary skill in the art who has read the disclosures of both Martin and Hagerstein to modify the system of Martin by centralizing the protocol determining circuitry in Martin's cache controllers into the network, as does Hagerstein.

23. The motivation for doing so is taught by Hagerstein on Page 4, line 58 – Page 5, line 2, namely that a centralized coherence transformer allows external processing elements that may have different protocols or bus speeds to access the system. Additionally, centralizing the circuitry significantly decreases the amount of circuitry needed to realize the use of the system, because the circuitry does not need to be duplicated for each processing element.

24. Therefore, it would have been obvious to combine the centralized coherence transforming circuitry of Hagerstein with the system of Martin, for the benefits above, to obtain the invention as specified in claim 13.

25. **As for claim 14**, Martin further teaches:

- A coherency mode unit (26, Fig. 1) configured to store an indication (42, Fig. 4; see also Pg. 3, Par. 57) to control whether a given coherency request is transmitted through said network according to a directory protocol or a broadcast protocol (Pg. 3, Par. 52). (While Martin does not name this unit a coherency mode storage unit, the cache controller he discloses performs the function of the mode unit disclosed by the instant application.)

26. Claims 8-10 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martin and Hagerstein as applied to claims 7 and 17 above, and further in view of Hagersten, US Patent 5,887,138.

27. As for the limitations of claims 8-10, Martin teaches all the limitations of claim 7 as described above. Martin additionally teaches that his mode storage unit stores an

indication (42, Fig. 4) to control whether coherency requests are transmitted through the network by a broadcast protocol or by a directory protocol (Pg. 3, Par. 57; Pg. 3, Par. 52). He teaches that, based on the indication, selected coherency requests are transmitted through the network by a directory protocol, and other coherency requests are transmitted through the network by a broadcast protocol. (The limitation of claim 9 in the instant application)

28. Martin, however, does not expressly teach that the coherency mode storage unit stores a plurality of *additional indications* to control which protocol should be used nor that an address of the request is one of the indications used to dictate the transmission protocol, as is claimed in claims 8 and 10.

29. **Hagersten, US Patent 5,887,138, does teach these limitations, disclosing** a multiprocessing computer system which includes a plurality of processing units (16, Fig. 1) with individual caches (18, Fig. 1), a shared memory (22, Fig. 1; also 36, Fig. 1A and 46, Fig. 1B), a point to point network (14, Fig. 1; also Col. 7, line 10) connecting the components, and a system interface (i.e., mode storage unit) which determines the transmission protocol (24, Fig. 1; Fig. 3; Col. 5, lines 18-24). Hagersten's system uses multiple coherency protocols depending on several indications, including whether a coherency request is directed toward a local or global address. Hagersten discloses that his system interface uses several indications to determine the protocol used, namely:

- Whether the address is local or global (Col. 5, lines 21-25);

- Whether there is a copy of the requested memory block in additional local memories in other global units (Col. 5, lines 21-25); and
- The access rights of the unit in question. (Col. 16, lines 22-28)

30. Hagersten discloses that his system interface stores:

- Translations from local to physical addresses, comparing several bits from the requested address to information stored in the interface (Col. 13, line 59 to Col. 14, line 3); and
- Information in an MTAG table (68, Fig. 3) that is used to determine access rights.

These indications are used in the determination of the protocol (Col. 16, lines 10-25).

31. Martin and Hagersten are analogous art because they are from the same field of endeavor, namely multiprocessing systems that use multiple and differing coherency protocols based on certain situations in an effort to reduce request latency and reduce network congestion.

32. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Martin to include the storage of multiple indications for protocol differentiation based on local / global address.

33. The suggestion for doing so is taught by Hagersten, on Col. 4, lines 20-50. The distributed memory architecture format sometimes used for multiprocessor systems can cause network congestion, creating a bottleneck. When a processor accesses a portion of memory that is not local to the processor's own node, it must create some network traffic. As lines 32-40 note, coherence requests directed to a shared memory segment

local to the processor's own node operate at a much higher bandwidth than requests directed over the network to a memory segment that is not local. Therefore, it would have been obvious to try to find a way to decrease the disadvantage that non-local coherence requests experience. A logical conclusion would be that the protocols that work well for local requests might not work well for non-local requests, because they create a bandwidth problem. Martin, in Page 1, Par. 7, notes that certain protocols that work quickly for small systems are not as desirable for large systems because they create a lot of network traffic, and that other protocols, while slower and more complex, (lines 3-4) use less bandwidth and would be better for use in non-local requests sent over a network.

34. Therefore it would have been obvious to modify the system of Martin by adding the limitations of Hagersten described above to create a system that has the advantage of quick request completion for both local addresses and non-local addresses, to obtain the invention as specified in claims 8-10.

35. As for the limitations of claims 18-20, Martin teaches all the limitations of claim 17 as described above. Martin additionally teaches that his mode storage unit stores an indication (42, Fig. 4) to control whether coherency requests are transmitted through the network by a broadcast protocol or by a directory protocol (Pg. 3, Par. 57; Pg. 3, Par. 52). He teaches that, based on the indication, selected coherency requests are transmitted through the network by a directory protocol, and other coherency requests are transmitted through the network by a broadcast protocol. (The limitation of claim 19 in the instant application)

36. Martin, however, does not expressly teach that the coherency mode storage unit stores a plurality of *additional indications* to control which protocol should be used nor that an address of the request is one of the indications used to dictate the transmission protocol, as is claimed in claims 18 and 20.

37. **Hagersten, US Patent 5,887,138**, does teach these limitations, disclosing a multiprocessing computer system which includes a plurality of processing units (16, Fig. 1) with individual caches (18, Fig. 1), a shared memory (22, Fig. 1; also 36, Fig. 1A and 46, Fig. 1B), a point to point network (14, Fig. 1; also Col. 7, line 10) connecting the components, and a system interface (i.e., mode storage unit) which determines the transmission protocol (24, Fig. 1; Fig. 3; Col. 5, lines 18-24). Hagersten's system uses multiple coherency protocols depending on several indications, including whether a coherency request is directed toward a local or global address. Hagersten discloses that his system interface uses several indications to determine the protocol used, namely:

- Whether the address is local or global (Col. 5, lines 21-25);
- Whether there is a copy of the requested memory block in additional local memories in other global units (Col. 5, lines 21-25); and
- The access rights of the unit in question. (Col. 16, lines 22-28)

38. Hagersten discloses that his system interface stores:

- Translations from local to physical addresses, comparing several bits from the requested address to information stored in the interface (Col. 13, line 59 to Col. 14, line 3); and

- Information in an MTAG table (68, Fig. 3) that is used to determine access rights.

39. These indications are used in the determination of the protocol to be used (Col. 16, lines 10-25)

40. Martin and Hagersten are analogous art because they are from the same field of endeavor, namely multiprocessing systems that use multiple and differing coherency protocols based on certain situations in an effort to reduce request latency and reduce network congestion.

41. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Martin to include the storage of multiple indications for protocol differentiation based on local / global address.

42. The suggestion for doing so is taught by Hagersten, on Col. 4, lines 20-50. The distributed memory architecture format sometimes used for multiprocessor systems can cause network congestion, creating a bottleneck. When a processor accesses a portion of memory that is not local to the processor's own node, it must create some network traffic. As lines 32-40 note, coherence requests directed to a shared memory segment local to the processor's own node operate at a much higher bandwidth than requests directed over the network to a memory segment that is not local. Therefore, it would have been obvious to try to find a way to decrease the disadvantage that non-local coherence requests experience. A logical conclusion would be that the protocols that work well for local requests might not work well for non-local requests, because they create a bandwidth problem. Martin, in Page 1, Par. 7, notes that certain protocols that

work quickly for small systems are not as desirable for large systems because they create a lot of network traffic, and that other protocols, while slower and more complex, (lines 3-4) use less bandwidth and would be better for use in non-local requests sent over a network.

43. Therefore it would have been obvious to modify the system of Martin by adding the limitations of Hagersten described above to create a system that has the advantage of quick request completion for both local addresses and non-local addresses, to obtain the invention as specified in claims 18-20.

44. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Martin and Hagerstein as applied to claim 1 above, further in view of Higuchi et al, US 5,774,731, hereinafter Higuchi.

45. Martin discloses the limitations of claim 1, as above.

46. Martin, however, does not expressly disclose that the network is implemented with a plurality of address switches.

47. Higuchi discloses a multiprocessing system, with the processing subsystems (2, Fig. 1A) interconnected via a network (1, Fig. 1A). The network of Higuchi is implemented with a plurality of address switches (see EX00-33, Fig. 2; also Col. 9, lines 60-67), thereby creating a point-to-point connection between the nodes.

48. Higuchi and Martin are analogous art because they are from the same area of endeavor, namely multiprocessing systems which utilize a point-to-point network to interconnect processing subsystems.

49. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the network of Higuchi in the system of Martin.

50. The motivation for doing so is disclosed by US 5,822,605 to Higuchi et al., (hereinafter "the '605 patent"), which is incorporated by reference in Higuchi's '731 patent. In Col. 4, lines 30-55 of the '605 patent, it is taught that the network allows rapid message transfer while avoiding deadlock, which is advantageous.

51. Therefore, it would have been obvious to combine Higuchi with Martin for the benefit of avoiding deadlock, to obtain the invention as specified in claim 11.

Allowable Subject Matter

Claim 12 is allowed. The prior art does not teach the combination including the negative limitation that the coherency request is routed "only to said directory" if the block is a point-to-point mode block.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. **Phelps, US 5,966,729**, discloses a multiprocessor system which includes both broadcast and directory coherence requests. The system includes a switch connecting the clients, and a central mode directory determining the transmission protocol.

Khare, US 6,810,467, teaches a multinode coherence system which includes a central switching device with a plurality of ports, to which the nodes are coupled.

Quatch, US 2004/0117561 A1, discloses a multi-client system with a centrol coherence switch. The switch receives point-to-point coherence requests from the clients and issues second requests based on a mode filter which acts as a directory. A further indication changes the mode so that the second requests are issued under a broadcast protocol instead of a directory protocol.

Deneroff, US 2005/0053057 A1, discloses a multi-nodal coherence system with a central network switch with individual ports. Coherence requests are routed from node to node, with the individual nodes not able to snoop the network.

Hagersten et al., US 5,887,138, Brown et al., US 2004/0059877, Kalla, US 2002/0138698, Weber, US 2001/0013089, Luick et al., US 6,088,769, Carpenter et al., US 6,081,874, and Bilir et al., ISCA '99 ("Multicast Snooping), all discuss hybrid cache coherence protocols, which use different protocols depending on the circumstances.

Gaither et al., US 6,868,481 and US 2003/0028730, teach a global coherence filter or GOTL, which holds an indication for certain cache lines. Based on this indication, different coherence protocols may be used. Gaither also discusses distributed GOTL and common GOTL, and their relative benefits.

Natarajan et al., "Survey on Cache Coherence", discuss hybrid cache protocols including broadcast/directory hybrids.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse Diller whose telephone number is (571) 272-4173. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JD

Brian R. Peugh
Primary Examiner